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# Modulation of electronic properties of tin oxide nanobelts via thermal control of surface oxygen defects

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## Abstract

Nanomaterials made from binary metal oxides are of increasing interest because of their versatility in applications from flexible electronics to portable chemical and biological sensors. Controlling the electrical properties of these materials is the first step in device implementation. Tin dioxide (SnO<sub>2</sub>) nanobelts (NB) synthesized by the vapor–liquid–solid mechanism have shown much promise in this regard. We explore the modification of devices prepared with single crystalline NBs by thermal annealing in vacuum and oxygen, resulting in a viable field-effect transistor (FET) for numerous applications at ambient temperature. An oxygen annealing step initially increases the device conductance by up to a factor of 10<sup>5</sup>, likely through the modification of the surface defects of the NB, leading to Schottky barrier limited devices. A multi-step annealing procedure leads to further increase of the conductance by approximately 350% and optimization of the electronic properties. The effects of each step is investigated systematically on a single NB. The optimization of the electrical properties of the NBs makes possible the consistent production of channel-limited FETs and control of the device performance. Understanding these improvements on the electrical properties over the as-grown materials provides a pathway to enhance and tailor the functionalities of tin oxide nanostructures for a wide variety of optical, electronic, optoelectronic, and sensing applications that operate at room temperature.

Keywords: nanobelt, field-effect transistor, annealing, tin dioxide, sensing

(Some figures may appear in colour only in the online journal)

## Introduction

Utilization of semiconducting nanostructures has become commonplace in many applications of semiconductor microelectronics. Traditionally, these nanostructure-based electronics are often produced from top-down processes which are limited by the minimum resolution of common lithographic and etching techniques [1, 2]. Furthermore, the top-down processes usually begin with a single substrate whose properties are modified in the device fabrication. More recently, the bottom-up assembly scheme based on pre-synthesized nanocomponents has attracted much interest. The

nanocomponents such as Si nanowires [3–5] and SnO<sub>2</sub> nanobelts (NBs) [6] as in this work afford the bottom-up scheme many advantages including control of their crystallinity and electronic properties. These devices have found applications outside the realm of electronics. For example, field-effect transistors (FETs) with semiconducting nanostructure channels have been demonstrated as effective gas [7–10], pH [11], and biological sensors [12–14]. SnO<sub>2</sub> is typically demonstrated as efficient gas sensors at elevated temperatures [7, 15, 16], but should be functional at room temperature to be compatible with the majority of chemical and biomolecular sensing applications. This study provides a

pathway for consistent production of functional nano devices based on this important sensor material.

We choose to focus on manipulation of quasi-one dimensional structures because they offer a range of benefits over their larger dimensional counterparts. Importantly, the dimensionality is consistent with the size of the desired analyte; detection of individual target molecules or species bound to the channel surface is theoretically possible [17]. The quantum confinement in one dimension is important for an effective turn-off of the FET with minimal molecule or species concentrations in real-time sensing applications [18].

Mass synthesis of single crystalline quasi-1D nanomaterials is often carried out via chemical vapor deposition of a source material in a well-controlled environment [19, 20]. Materials commonly used, such as silicon, can be controllably doped by introducing dopant sources as an additional precursor gas during the growth [3, 5, 21]. We focus on vapor-liquid-solid (VLS) grown oxides, which offer the advantages of self-doping and the possibility of being modified post-growth by thermal annealing or surface modification procedures. In fact, we present in this work the utility of post-growth annealing of SnO<sub>2</sub> NBs to optimize the source/drain contacts at the metal-semiconductor interface and to tune the electronic characteristics of the channel in order to produce optimal room temperature FETs based on the oxide nanomaterials.

Transparent conducting oxides (TCOs) are a family of material that have attracted interest from the scientific and technological communities for their unique semiconducting properties [22]. The transparency of TCOs at nanoscale thicknesses has already found various applications including solar cells and electronic displays [23]. Due to the robust mechanical properties of these semiconductors, TCOs are being exploited as suitable materials in the increasingly popular development of flexible electronics and solar cells [24, 25]. Highly conductive, optically transparent materials are ideal for use as micro-contacts on solar cells [26–28]. Optically transparent materials generally have large fundamental band gaps and exhibit insulating behavior; however, it has been demonstrated that TCOs exhibit high electrical conductivities [29]. It is generally accepted that the main contributor to conductance is the presence of oxygen vacancies [30] in the material. Since the conductivity comes from a defect inherent in the material, our work supports the possibility to modify the conductivity by altering the number of dopants via thermal treatments, in contrast to silicon NWs which have a fixed number of dopants determined by the growth procedures.

In our work, we note that devices from as-grown SnO<sub>2</sub> NBs do not show any measurable electrical conductance. Previous work on ZnO [31] and SnO<sub>2</sub> [32] has demonstrated that a thermal treatment does in fact have a significant impact on device characteristics, however, the literature is lacking in detailed studies into the effects of thermal annealing on the electrical properties of TCOs. It has been suggested that at temperatures above 900 °C there is a structural change in the chemical makeup of SnO<sub>2</sub> [33]. A defect region of up to 1.4 nm at the surface has been observed in other NBs of

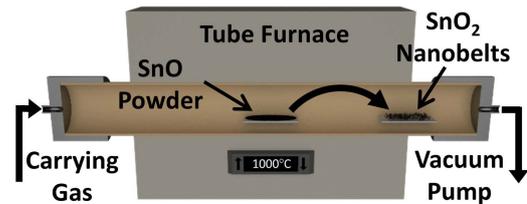


Figure 1. Schematic of the NB growth apparatus.

similar composition grown by different methods [34]. However, our thermal processes are carried out at relatively low temperatures, below 600 °C, and therefore changes are attributed to modification of the surface defects supported by our photoluminescence results.

In order to implement nanoscale TCOs in functional devices, the electrical properties must be examined and optimized. In this work, we synthesize SnO<sub>2</sub> NBs and tune the electronic transport properties with application in FETs as our main focus, but these results could also have important impacts on the development of transparent coatings and contacts for solar cells. The as-grown products are subjected to a thermal annealing procedure to increase their conductivities and ensure that metallization produces Ohmic contacts with electrical properties tunable to the needs of a variety of applications. We observe an increase in device conductance by a factor of 10<sup>5</sup> after thermal treatment of the NB before metallization with Cr/Au contacts. In the case of FETs, it is also important to ensure the material has ‘on/off’ current ratios that are orders of magnitude for efficient detection. In our samples, we demonstrate enhancement of the ‘on/off’ ratios to 3 orders of magnitude.

## Experimental methods

The NBs used in this work were synthesized in a horizontal tube furnace (Lindberg, Blue M) from SnO (99.99% pure, metal basis, Alfa Aesar). The source powder was loaded onto an alumina (Al<sub>2</sub>O<sub>3</sub>) substrate and transferred to the center of an Al<sub>2</sub>O<sub>3</sub> tube. A schematic is shown in figure 1. Several deposition substrates were placed downstream to collect the product. The growth was carried out at 1000 °C for 2 h. After initial evacuation to below 50 mTorr, an Ar gas flow at a rate between 50 and 500 sccm was introduced through the chamber and a steady pressure of 300 Torr was achieved. The growth occurs via the self-catalyzed VLS mechanism [35, 36]. After growth, the NBs were suspended in isopropyl alcohol via sonication and stored for later use. The NBs were dispersed dropwise (~10 μl) on a wafer (NOVA Electronics) consisting of a heavily p-doped silicon substrate (500 μm) with 250 nm of SiO<sub>2</sub> thermally grown on top. At this point the devices are ready for pre-fabrication treatment to modify the surface properties which have been found to profoundly impact the electrical characteristics of the NB and resulting device.

Several different annealing procedures have been tested. Typically, the SnO<sub>2</sub> NBs were annealed in either a vacuum

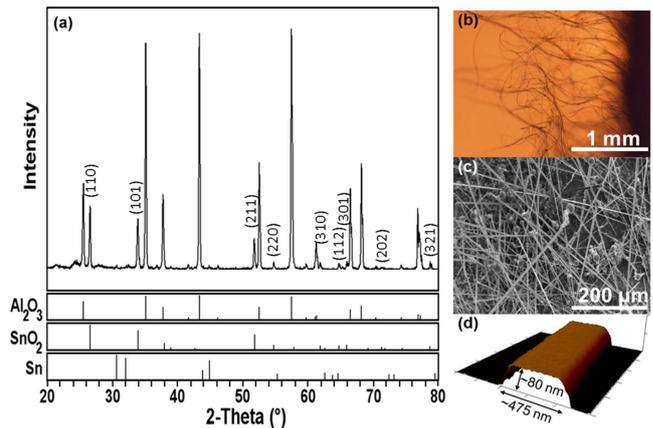
environment reaching the order of 50 mTorr, a pure O<sub>2</sub> environment maintained at ~760 Torr, or via a specific three-step procedure to be described in detail below involving these conditions. The annealing was carried out in a set-up similar to that for the growth with a clean alumina tube to limit contamination. In each case, the tube was first evacuated to ~50 mTorr to remove contaminants and ensure a clean environment for the annealing. The thermal annealing steps were carried out in different sequences to compare the effects. The annealing procedure contains three steps. The first is at 250 °C in vacuum at ~50 mTorr for 1 h. This is followed by a 3 h anneal at 600 °C in 760 Torr O<sub>2</sub>. We have achieved similar results by using a regulator to fix the pressure at 760 Torr or by opening the downstream end of the tube to the ambient environment. The oxygen flow rate was maintained at 50 sccm when a regulator was employed and kept at 125 sccm when the tube was opened to the environment. The difference in flow rate did not significantly affect the annealing results. Finally, the sample is annealed in vacuum at 250 °C for 3 h at the base pressure of around 50 mTorr.

After the annealing process, the device fabrication was immediately carried out to ensure minimal degradation of the surface due to environmental exposure. A single NB was identified by optical microscopy. Utilizing a pre-deposited alignment grid, we map the location of the NB. Either photolithography or electron beam lithography was used to define at least four contacts on the NB or NB section to be tested. Next, thermal evaporation of Cr/Au (5 or 10/100 nm) was performed for metallization. A delicate lift-off step in acetone without any sonication yields the final device. We also test, stepwise, the annealing procedure on an individual NB by subsequent annealing and metallization along the length or cutting the NB into sections with reactive ion etching in a CCl<sub>2</sub>F<sub>2</sub>/O<sub>2</sub> plasma.

Bundles of NBs were analyzed by powder x-ray diffraction (XRD) on the growth substrate to confirm the product composition. Individual NBs were measured by atomic force microscopy (AFM) to help identify their geometrical characteristics and to verify the claim that they are nanoscale. Photoluminescence spectra on individual NBs were obtained using a mercury lamp with an excitation filter of 330–380 nm (3.3–3.8 eV) to probe the presence of surface oxygen defects. The products both before and after annealing were characterized by conventional two- and four-probe measurements to determine their conductivity and contact resistance. The efficacy of the devices as FETs was verified by determining the gate dependence of the channel using the typical backgate geometry with the p+-doped silicon as the backgate. Measurements in this manuscript are carried out in either ambient or vacuum environment as indicated and at room temperature.

## Results and discussion

The SnO<sub>2</sub> NBs were synthesized under the given parameters with varying degrees of success for flow rates between 50 and 500 sccm, generally with increasing yield at higher flow rate. Our best results were obtained using a flow rate of 200 sccm,

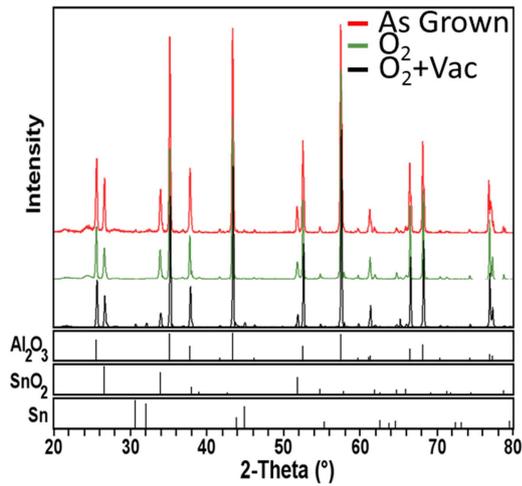


**Figure 2.** Bulk characterization of the as-grown NBs by (a) XRD highlighting the peaks of rutile SnO<sub>2</sub>, (b) optical microscopy showing the ultra-long lengths of the product, (c) SEM with visible seed particles as evidence of the VLS growth mechanism, and (d) AFM with measured 475 nm and 80 nm width and thickness respectively, corresponding to a 5.9:1 aspect ratio.

producing a significant amount of the white/gray wool-like clusters occurring primarily at the location in the growth tube near the edge of the tube furnace. This indicates a likely dependence on the cooling of the growth environment downstream from the source powder as an important factor in NB growth, and is supported by the literature [37]. One may be able to increase the yield or better control the geometrical dimensions of the product with a multi-zone furnace or another method to control the temperature gradient of the growth environment. In this work, we focus on the post-growth annealing which we believe to be a factor independent of the as-grown product based on similar results obtained with different growth parameters.

Figure 2 shows the structural properties of the NBs as measured with XRD, optical microscopy, scanning electron microscopy (SEM), and AFM. The XRD results verify that the SnO<sub>2</sub> NBs exhibit the expected rutile structure: the peaks in figure 2(a) are matched from a database to the rutile form of SnO<sub>2</sub>, cassiterite [38], and background peaks from the alumina growth substrate. The products were observed to be in excess of 100 μm, in some cases up to millimeters long (figure 2(b)). We see evidence of the VLS growth mechanism in the SEM image (figure 2(c)) where the majority of NBs are terminated by a spherical seed particle consistent with previous work [9]. Maintaining a large width-to-thickness ratio ensures a large surface-to-volume ratio beneficial for sensing applications. We were able to fabricate NB FETs with typical NB thicknesses ranging between 30 and 150 nm and exhibited typical width-to-thickness ratios of between 5:1 and 10:1, but ultimately vary significantly. The NB shown in figure 2(d) has a width and thickness of approximately 475 nm and 80 nm, respectively, as measured by AFM. This gives a width-to-thickness ratio of 5.9:1.

The primary goal of this work is to examine the effects of thermal annealing on the SnO<sub>2</sub> NB and the resulting device. Two-probe measurements were taken to initially characterize the electrical conductance. XRD measurements on the as-

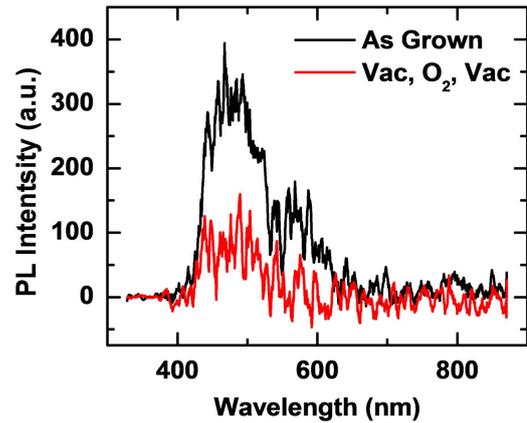


**Figure 3.** XRD spectra for bundles of the as-grown and thermally annealed NBs on the alumina growth substrate, showing peaks for alumina, SnO<sub>2</sub>, and Sn.

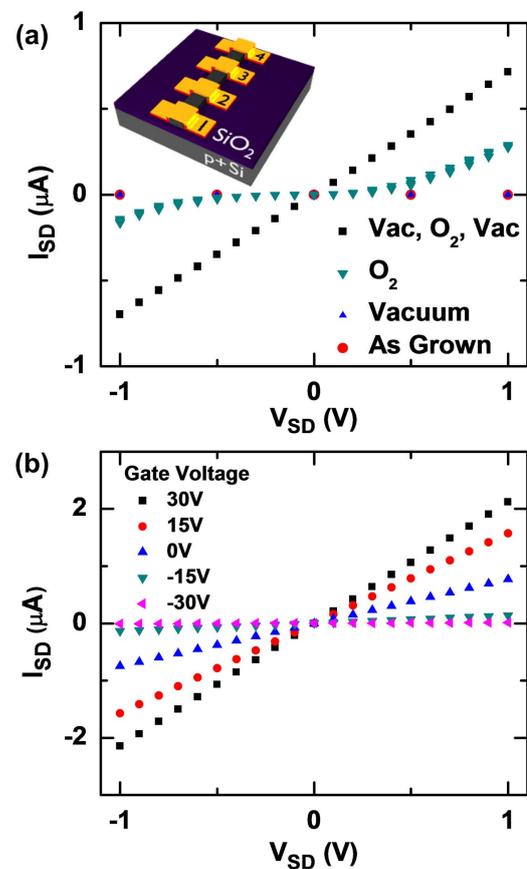
grown, oxygen, and combination oxygen/vacuum annealed samples are essentially identical (figure 3). We see the characteristic peaks of the tetragonal form of SnO<sub>2</sub>, alumina growth substrate, and small signals attributed to pure Sn. Particularly in the oxygen/vacuum annealed sample, we see some peaks from Sn, which could be from the unreacted seed particles found at the ends of the NBs. These XRD spectra were taken from different portions of the same growth and annealed separately. From the XRD, we surmise that the bulk properties of the NBs are not being affected by the thermal treatment.

Photoluminescence measurements were performed with a mercury lamp excitation source and excitation filter for 330–380 nm. The positions of individual NBs were identified optically in reference to an alignment grid pre-patterned on a glass substrate. This ensured that the same NB could be compared before and after annealing. The spectra taken on as-grown individual NBs reveal two broad luminescence peaks at about 480 nm (2.6 eV) and 600 nm (2.1 eV) shown in figure 4. These peaks, attributed to defect electronic states from surface oxygen vacancies [39, 40], are consistently reduced after the annealing process. This suggests a shift to a more stoichiometric surface which exhibits less band bending and therefore a smaller barrier at the metal–semiconductor interface [41], consistent with our understanding of the reason for the enhanced electrical properties.

It has been noted previously that similarly synthesized, as-grown NBs exhibit insulating behavior and must be subjected to a thermal annealing procedure for activation [32]. Electrical measurements taken on as-grown NBs support this observation (figure 5(a)), with measured electrical signals consistent with the minimal leakage current from the grounded gate electrode through the dielectric layer. Even at 10 V of source–drain bias ( $V_{SD}$ ) and zero gate potential, we observe  $I_{SD} \sim 1$  nA. We are unable to tune the n-type semiconducting channel to the ‘on’-state even with applied gate voltages as high as 30 V. Noting that the conductivity in TCOs is generally attributed to the presence of oxygen vacancies in the



**Figure 4.** Photoluminescence spectra for a single NB before and after the full annealing procedure.

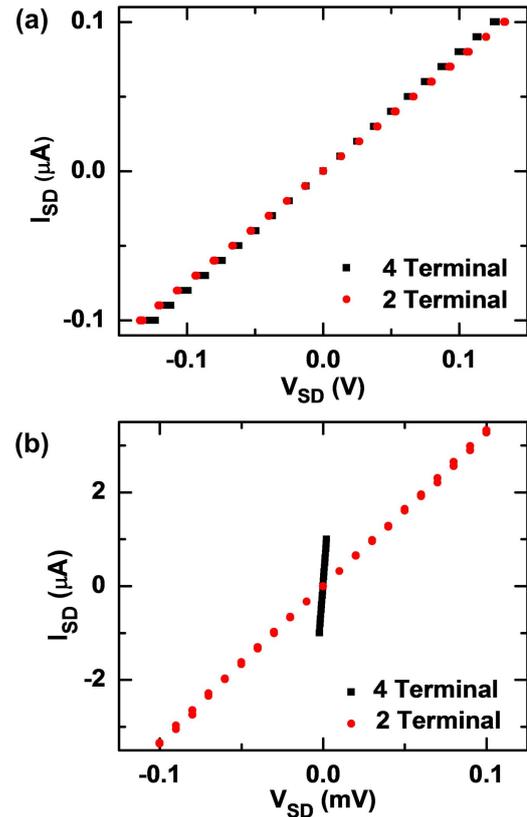


**Figure 5.** (a) Source–drain  $I$ – $V$  of four separate NB devices, showing the change in electrical properties arising from thermal annealing. Inset: device schematic. (b) The conductance modulation by an applied backgate potential between terminals 2 and 3 on the triple annealed device in (a) having an ‘on/off’ ratio greater than 2 orders of magnitude.

material, we try to increase the number of carriers in our material by annealing in a vacuum environment. We carry out the annealing at 250 °C for 3 h in a  $\sim 50$  mTorr environment. Performing this annealing step alone produces results identical in nature to those of the as-grown NBs with current on the order of hundreds of picoamps which is of the order of leakage current of our measurement set-up, and again we see

an inability to tune the device to the ‘on’-state with an applied gate potential. We find it necessary to perform an additional oxygen annealing step, in a  $\sim 760$  Torr oxygen environment for 3 h, to activate electrical conduction in the material and produce devices exhibiting current on the order of  $1 \mu\text{A}$  for 1 V source–drain bias. Samples subjected to only the  $\text{O}_2$  annealing exhibit  $I$ – $V$  characteristic indicative of back-to-back Schottky barriers. The conductance increases by up to 5 orders of magnitude compared to the as-grown material. These devices can be tuned from an effective ‘off’-state to an ‘on’-state, with maximum ‘on/off’ ratios of three orders of magnitude (data not shown). The increase in conductivity after oxygen annealing is at first counter-intuitive, but could be attributed to the reduction of defects along the channel, similar to results obtained on ZnO [42]. We have observed in similar devices that the gate modulation after  $\text{O}_2$  annealing is sufficient for sensing experiments; however, the reduction in the device conductance with decreasing gate voltage likely is dominated by the modification of the Schottky barrier at the interface as opposed to the reduction of carrier concentration in the channel material [43]. The effect from the Schottky barrier is expected to be exponentially related to the barrier,  $I \propto \exp(-q\phi_B/kT)$  where  $I$  is the current,  $q$  is the fundamental charge,  $\phi_B$  is the barrier height,  $k$  is the Boltzmann constant, and  $T$  is the temperature. In contrast, the channel effect is expected to be linear with the carrier concentration,  $\sigma = nq\mu$ , where  $\sigma$  is the conductivity,  $n$  is the carrier density, and  $\mu$  is the carrier mobility.

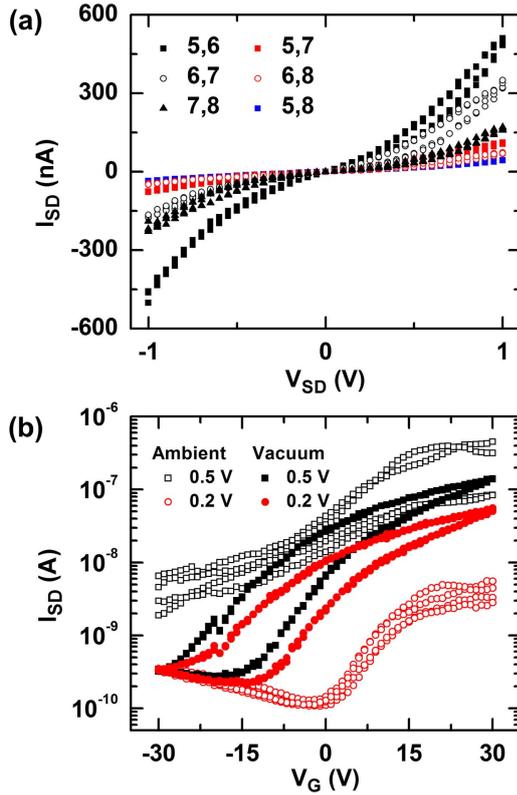
We are able to reliably fabricate Ohmic devices with a combination of the vacuum and oxygen annealing procedures. Our process consists of three steps: a vacuum annealing to help provide a clean environment through the removal of water and other potential adsorbates, an oxygen annealing that we believe contributes to the reduction of surface defects on the material which may result in a reduction in contact resistance and/or increased carrier mobility, and a second annealing in vacuum that serves to tune the number of oxygen vacancies and thus the conductance in the channel. It is possible that this tuning comes from a desorption of oxygen from the surface, leaving defect states which may be populated by diffusion of oxygen from the bulk to the surface, and thus a diffusion of vacancies from the surface to the bulk [41]. We see in figure 5(a) that through these steps, we obtain devices that exhibit linear  $I$ – $V$  relationships. The linear region conductances of the as-grown, vacuum annealed, oxygen annealed, and triple annealed devices with equal channel lengths are  $2.0 \times 10^{-12}$ ,  $5.5 \times 10^{-12}$ ,  $2.0 \times 10^{-8}$ , and  $7.0 \times 10^{-7}$  S, respectively. We explore the modulation of the conductance via an applied backgate potential and present our results in figure 5(b). For this device the ‘on/off’ ratio is 2 orders of magnitude where the conductance between terminals 2 and 3 is reported as  $1.0 \times 10^{-8}$  and  $2.1 \times 10^{-6}$  S for  $V_G = -30$  and 30 V, respectively. It is possible that the ‘on/off’ ratio is limited by the minimum ‘off’ current achievable with our gate dielectric and measurement apparatus and not the real ‘off’ current of the NB. For triple annealed devices, the contacts are verified to have little effect on the electronic properties of the device by comparing the two terminal



**Figure 6.** (a) Comparison of two- and four-terminal  $I$ – $V$  relations showing that the contacts only contribute 5.5% to the device resistance and (b) a device with an exceptionally conducting channel with comparatively large contact resistance, still operating in the Ohmic regime, where the contacts contribute 92% of the device resistance.

measurements to four-terminal measurements where the current is applied through the outermost leads and the voltage is measured between the innermost leads. Figure 6(a) demonstrates the similarity in the two measurements with conductances of  $7.51 \times 10^{-7}$  and  $7.95 \times 10^{-7}$  S for the two- and four-terminal schemes respectively. The contacts contribute to 5.5% of the resistance, and assuming they have equal contribution, are extracted to be  $36.9 \text{ k}\Omega$ . For most linear devices we observed a significant overlap between the two measurements and the contacts are determined to contribute  $<6\%$  of the total device resistance. However, it is possible to have Ohmic contact resistance much larger than the channel resistance when the channel is extremely conductive as in figure 6(b). Here the channel resistance is  $2.2 \text{ k}\Omega$  and each of the contact resistances are  $14.1 \text{ k}\Omega$ , meaning the contacts are roughly 92% of the device resistance.

To this point, we have demonstrated the value of annealing the NBs by this specific process to produce FETs with desirable characteristics, however, a precise quantitative comparison between devices is still lacking because of the need to perform the experiments on separate FETs based on different NBs subject to different annealing processes. To limit the variability introduced by the use of multiple devices that can arise from geometrical or experimental procedures, we develop a method for testing the annealing and device



**Figure 7.** (a) Two-terminal  $I$ - $V$  relation of a NB device subjected to two-step 1 h, 250 °C vacuum and 3 h, 600 °C O<sub>2</sub> anneal showing back-to-back Schottky contacts. (b) Transfer curves at 0.5 V (black) and 0.2 V (red) source-drain biases in ambient (open) and vacuum (solid) environments.

characteristics on a *single* oxide NB in a stepwise fashion. We implemented two methods that show qualitatively identical results. In our first experiments, a single NB was identified by optical microscopy and, with the help of e-beam lithography and reactive ion etching, we were able to cut the NB into 4 equal sections. These sections were cut to prevent any migration of the contact metal during thermal treatment that could complicate analysis. In subsequent experiments, we forego the segmentation by RIE and the initial measurements on the as-grown material.

In figure 7, we present the electrical properties of a NB after both a 250 °C vacuum anneal for 1 h and a 600 °C oxygen anneal for 3 h. We took care to perform the annealing and subsequent metallization as quickly as possible (within a few hours) of the section under scrutiny. This helps to limit any effect on the surface defects from the environment adversely affecting the fabrication. We do not see any conductance above the gate leakage of the measurement set-up when metallizing the as-grown portion of the NBs, so this step is skipped. The  $I$ - $V$  relation in figure 7(a), typical of two back-to-back Schottky junctions, is predominantly limited by the contact. We can appreciate the large increase in conductance from the vacuum annealed to oxygen annealed NBs. The conductance per unit length determined by fits to the linear region is  $1.41 \times 10^{-4} \text{ S nm}^{-1}$  and  $9.21 \times 10^{-2} \text{ S nm}^{-1}$  for the vacuum and oxygen annealed section, respectively.

This more than two orders of magnitude increase in the conductance evidences the effect the oxygen annealing has on the NB. Typically, this annealing step results in weak Schottky barrier-like  $I$ - $V$ s, approaching Ohmic-like contact in a limited number of samples. It is common to have hysteresis in the source-drain  $I$ - $V$  curves, likely due to the effects of humidity or water on the device characteristics. These hysteresis loops have consistently diminished when measurements are taken in a vacuum environment.

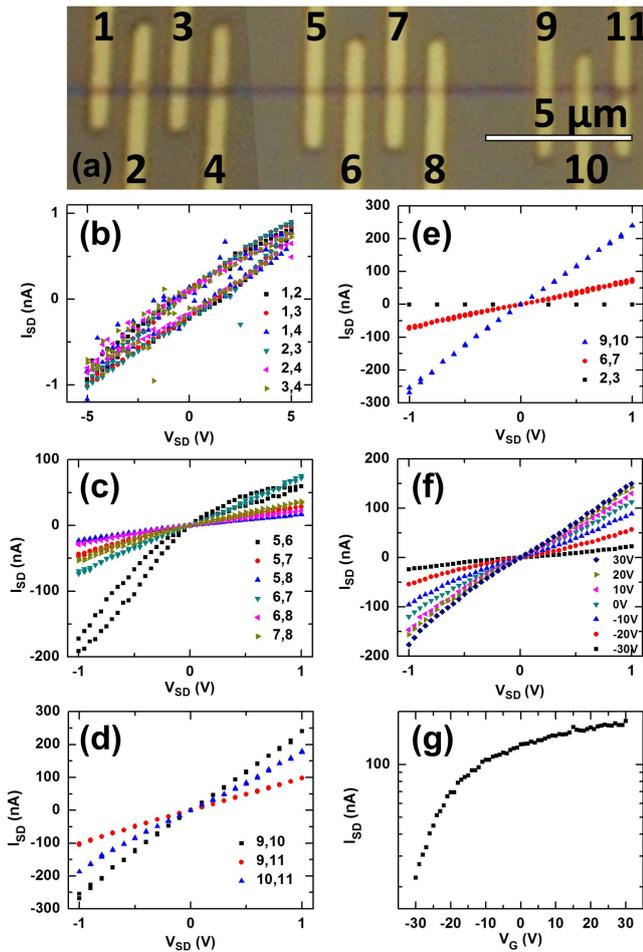
We take this sample and perform gating measurements in both ambient and vacuum to contrast the device in a humid environment to a dark,  $\sim 1$  Torr environment after the oxygen annealing. Figure 7(b) shows the device response to an applied backgate potential over a 60 V range at source-drain biases of 0.5 and 0.2 V under both conditions. Contrasting the humid from vacuum environment, we first note the repeatability of multiple gate voltage sweeps clearly indicating a benefit of working with the device in vacuum. In ambient, the ‘on’ current of the device decreases with consecutive sweeps, possibly due to an electrical annealing of the surface, forcing adsorbates from the material. While there is little hysteresis in the ambient sweep, a pronounced hysteresis arises under vacuum. It is not currently clear why an increase in the gating hysteresis would appear under vacuum, but we can surmise that the effect is possibly related to the concentration of water, where it acts as a charge trap at low concentrations, but not high concentrations [44]. Previous work has shown the hysteresis could be reduced by appropriate control of the gate voltage sweep range or adequate passivation of the material surface [45] or gate voltage sweep rate [46]. We observe similar ‘on/off’ ratios for both environmental conditions of about  $10^2$ , but the ratio in vacuum is consistently larger. The threshold voltage,  $V_T$ , for 0.2(0.5) V source-drain bias is  $-2$  ( $< -30$ ) V for ambient. In vacuum the threshold voltage shifts to  $-30$  ( $< -30$ ) V or  $-15$  ( $-20$ ) V for negative to positive or positive to negative sweep directions, respectively. Using the relations presented by Huang *et al* [47] for a nanobelt-shaped FET with an applied backgate potential, we estimate the field-effect mobility,  $\mu_{\text{eff}}$ , as

$$\mu_{\text{eff}} = \left( \frac{dI_{\text{SD}}}{dV_{\text{g}}} \right) \frac{Lh}{\epsilon\epsilon_0 V_{\text{SD}} W},$$

where  $\frac{dI_{\text{SD}}}{dV_{\text{g}}}$  is found from the linear portion of the gate dependence,  $L$  is the channel length,  $W$  is the channel width,  $h$  is the dielectric thickness,  $\epsilon$  is the dielectric constant of SiO<sub>2</sub>, and  $\epsilon_0$  is the permittivity of free space. Using  $\epsilon = 3.9$ ,  $L = 800 \text{ nm}$ ,  $W = 300 \text{ nm}$ ,  $h = 250 \text{ nm}$ ,  $t = 100 \text{ nm}$ , we find  $\mu_{\text{eff}} \sim 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  regardless of  $V_{\text{SD}}$  or environment. The carrier concentration,  $n$ , can be found from

$$n = \frac{V_T \epsilon \epsilon_0}{qTh},$$

where  $T$  is the NB thickness.  $n$  is determined to be on the order of  $10^{17} \text{ cm}^{-3}$  in vacuum. It should be noted that there is significant error in the determination of  $V_T$  in ambient when  $V_{\text{SD}} = 0.5 \text{ V}$  and that the carrier concentration in ambient for



**Figure 8.** (a) A composite optical image of the final device after each sequential annealing and metallization procedure ( $5\ \mu\text{m}$  scale bar). Two terminal  $I$ - $V$  relation of the contact combinations on each section after the sequential (b) 1 h,  $250\ ^\circ\text{C}$  vacuum, (c) 3 h,  $600\ ^\circ\text{C}$   $\text{O}_2$ , and (d) 3 h,  $250\ ^\circ\text{C}$  vacuum thermal treatment. (e)  $I$ - $V$  relationship of two consecutive contacts taken from (b) to (d). (f) Gate modulation after final vacuum annealing for terminals 9–10, which have  $\sim 800\ \text{nm}$  separation. (g) Transfer characteristics from (f).

$V_{\text{SD}} = 0.2\ \text{V}$  is one order of magnitude less than in vacuum. This disparity can potentially be explained by the instability in surface adsorbates in a humid environment where  $\text{H}_2\text{O}$  or adsorbed  $\text{O}_2$  is likely driven off at larger biases. We see from the equation that a left-shift of the threshold voltage is indicative of an increase in carrier concentration for an n-type device. Our results are comparable to those on ZnO where vacuum induces a left-shift of  $V_T$  [48]. The vacuum environment could increase the presence of oxygen vacancies, consistent with an increase in carrier concentration. One could cause the threshold voltage to right-shift by reducing the gate dielectric thickness or possibly by increasing the contact separation to greater than  $\sim 800\ \text{nm}$  in this device.

Figure 8 exemplifies the effect of each of the individual steps of the annealing procedure on the device characteristics. Figure 8(a) shows the final device after metallization of each section from combined optical images with the terminal designations labeled. The contacts from previous sections are

typically destroyed as a result of annealing subsequent sections, so measurements between the two sections are not possible. Figure 8(b) shows the two terminal  $I_{\text{SD}}$  versus  $V_{\text{SD}}$  of the vacuum annealed (carried out at  $250\ ^\circ\text{C}$  for 1 h at  $\sim 50\ \text{mTorr}$ ) section, displaying currents on the order of hundreds of picoamps for a relatively large 20 V range of  $V_{\text{SD}}$ . The  $I$ - $V$  curves are independent of the channel separation or contact resistance, indicating that the measurement is between each individual drain contact and the gate. The hysteresis loop is most likely indicative of charge traps in the silicon dioxide dielectric layer than in the channel material itself [49]. Annealing at higher temperatures in vacuum could lead to increased conductance of the device, however at significant temperatures our device oxide is destroyed (identified by large gate leakage currents) and thus measurements of the channel are not realizable and therefore not applicable in this scheme. Figure 8(c) shows two-terminal conductance of the channel after subjecting the device to the  $600\ ^\circ\text{C}$   $\text{O}_2$  anneal at 760 Torr for 3 h. The conductance increases from  $1.57 \times 10^{-4}\ \text{S nm}^{-1}$  to  $5.76 \times 10^{-2}\ \text{S nm}^{-1}$  for the linear region of the vacuum and oxygen annealed sections, respectively. We see that the formation of Schottky contacts is not consistent along the length significantly affecting the two-terminal conductance (e.g. between terminals 5–6), but there is no clear trend to claim systematic evolution with length of the barrier. After annealing the NB in vacuum for the second time at  $250\ ^\circ\text{C}$  for 3 h, the  $I$ - $V$ s become linear below 1 V of source–drain bias (figure 8(d)). Moreover, the conductance per unit length now increases to  $1.97 \times 10^{-1}\ \text{S nm}^{-1}$ , a  $\sim 350\%$  increase from the oxygen annealed section. We attribute this increase in conductance to a tuning of the metal–semiconductor interface. If all of the contacts shared similar values for the contact resistance, terminals 9–10 and 10–11 should overlap. The fact that they do not overlap indicates a difference in contact resistance that we cannot extract with our measurements. This difference could be a result of some issue in metallization of a particular area arising from experimental complications. In figure 8(e) we plot the  $I$ - $V$ s for one pair of consecutive contacts with equal separations from each section to demonstrate graphically the evolution achieved from the annealing. After the vacuum annealing, we see a reduced gate modulation over the same range as the oxygen annealed section (figure 8(f)), however it is still more than one order of magnitude, within the range we are investigating (figure 8(g)), larger than previously reported [32] for the vacuum annealed NB. Using the previously defined relation, the field-effect mobility for a triple-annealed device increases to  $4\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$  from  $1\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ .  $V_T$  is shifted to less than  $-30\ \text{V}$  indicating that the density of carriers has increased with respect to the values determined from figure 7(b). However, we cannot accurately determine the density of carriers from our data range. Again, we can improve the gate response by choosing a more suitable wafer with a thinner dielectric and less charge traps or using the increasingly common extended gate or ionic gate scheme. This linear device, along with the Schottky device, provide useful pathways to fabricating tin dioxide FETs with

appropriate characteristics tailored for a variety of applications functional at room temperature.

## Conclusions

Rutile SnO<sub>2</sub> NBs were synthesized in the experimental growth environment using a variety of growth parameters. The as-grown NBs were found to be insulating; however, subjecting them to a thermal annealing process before metallization in oxygen activated the conductance of the NB devices, increasing it by a factor of 10<sup>5</sup>. In both Schottky and Ohmic-like devices, we observed the treated NBs to exhibit conductances in excess of 10<sup>-7</sup> S. We found that following the oxygen annealing with a vacuum annealing further increased the device conductance by 350%. With appropriate annealing, application of a backgate could tune the devices from an 'on'-state to an 'off'-state with an 'on/off' ratio of nearly 10<sup>3</sup> at room temperature. Our results provide useful guidelines for tailoring this important nano-scale sensor material for various electronic, optoelectronic, and sensing applications.

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## Author contributions

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## Notes

The authors declare no competing financial interest.

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